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SUITE 3100
PITTSBURGH, PA 15219-2502

EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	09/899,977	KEETH ET AL.	
	Examiner	Art Unit	
	MICHAEL T. TRAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70,71,100,120,135,136,152,167-188 and 203-208* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *71,135,136,174 and 175* is/are allowed.

6)☒ Claim(s) *70,100,120,152,167,172,173,176,185-188,203 and 205-208* is/are rejected.

7)☒ Claim(s) *168-171,177-184 and 204* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
AU 2827

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated June 14, 2006, claims 70, 71, 100, 120, 135, 136, 152, 167-188 and 203-208 are active in this application as a result of the cancellation of claims 1-69, 72-99, 101-119, 121-134, 137-151, 153-166 and 189-202.

Claim Rejections- 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 152, 203 and 205-208 are rejected under 35 U.S.C 102(b) as being anticipated by Keeth [U.S. Patent # 5,651,011].

With respect to claim 152, Keeth disclose, in figure 2, a method of placing a solid state memory device into a test mode, comprising: applying to the device a voltage outside the range of voltages used to represent logic signals [via 74], and while said

voltage is being applied; applying a specific combination of control signals to enable the receipt of a test enable key [via 22 of figure 1]; verifying the test enable key and confirming the presence of the applied voltage [via 26 of figure 1]; applying said specific combination of control signals to enable the receipt of at least one test mode key [see figure 4]; and decoding the test mode key to place the device in a test mode [see figure 4].

With respect to claim 203, Keeth disclose the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device – normal or supervoltage.

With respect to claim 205, Keeth disclose, in the Abstract and Detailed Description, the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

With respect to claim 206, Keeth disclose, in the Abstract and Detailed Description, the step of inputting a clear test mode key to take the device out of a test mode.

With respect to claim 207, Keeth disclose, in the Abstract and Detailed Description, said test mode keys are received as address information on column address lines.

With respect to claim 208, Keeth disclose, in the Abstract and Detailed Description, the steps of performing the test specified by the test mode key and outputting the test

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 70 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011].

With respect to claim 70, Hilley et al. disclose, in the figures and specification, a dynamic random access memory, comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching

data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd].

Hilley et al. disclose all of the above mentioned but is silent about the fact that there's a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices. However, this is not new. Keeth disclose that it is well known to have a plurality of voltage supplies [normal or super voltage] within a memory device for purposes of testing. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. memory circuit element's testing circuit to include the testing circuit as taught by Keeth, since the modification is merely a substitution of a functionally recognized equivalent element. Further, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

4. Claim 167 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011] and Sato et al. [U.S. Patent # 5,517,454].

Hilley et al. disclose, in the figures and specification, a dynamic random access memory, comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral

devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd]. Additonally, Keeth disclose, as stated above, a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices. Further, there exists rows and columns within the individual arrays within the memories of both Hilley et al and Keeth.

Hilley et al. and Keeth disclose all of the above mentioned but is silent about the fact that the dram has a sense amplifier. However, this is not new. Sato et al. disclose that it is well known to have sense amplifiers within a dram in order to convey data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. and Keeth memory circuit elements to include the sense amplifiers as taught by Sato et al., since the modification is merely a substitution of a functionally recognized equivalent element. Further, the sense amplifiers of Sato et al. not only improve the performance of the device, but also a necessity for the functionality of the device. Additionally, it is noted that it has been held that omission of an element and its function in a combination where the remaining

elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

5. Claims 172 and 173 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011] and Zagar et al. [U.S. Patent # 5,761,145].

Hilley et al. disclose, in the figures and specification, a dynamic random access memory, comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd]. Additonally, Keeth disclose, as stated above, a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices. Further, there exists rows and columns within the individual arrays within the memories of both Hilley et al and Keeth.

Hilley et al. and Keeth disclose all of the above mentioned but is silent about the fact that the dram has a capacity of 256 meg and that there exists redundant arrays to

replace any defective cells. However, this is not new. Zagar et al. disclose that it is well known to have a dram with a capacity of 256 meg as well as corresponding redundant cells to replace any defective normal cells. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. and Keeth memory circuit elements to include the memory capacity as taught by Zagar et al., since the modification is merely a substitution of a functionally recognized equivalent element. Additionally, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

6. Claim 100 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011].

With respect to claim 100, Hilley et al. disclose, in the figures and specification, a control unit for performing a series of instructions [memory controller - figure 2]; and a dynamic random access memory responsive to said control unit [banks coupled to the memory controller], said memory comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching

data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd].

Hilley et al. disclose all of the above mentioned but is silent about the fact that there's a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices. However, this is not new. Keeth disclose that it is well known to have a plurality of voltage supplies [normal or super voltage] within a memory device for purposes of testing. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. memory circuit element's testing circuit to include the testing circuit as taught by Keeth, since the modification is merely a substitution of a functionally recognized equivalent element. Further, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

7. Claim 176 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011] and Sato et al. [U.S. Patent # 5,517,454].

Hilley et al. disclose, in the figures and specification, a control unit for performing a series of instructions [memory controller - figure 2]; and a dynamic random access

memory responsive to said control unit [banks coupled to the memory controller], said memory comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd]. Additionally, Keeth disclose that it is well known to have a plurality of voltage supplies [normal or super voltage] within a memory device for purposes of testing. Further, there exist rows and columns within the individual arrays within the memories of both Hilley et al and Keeth.

Hilley et al. and Keeth disclose all of the above mentioned but is silent about the fact that the dram has a sense amplifier. However, this is not new. Sato et al. disclose that it is well known to have sense amplifiers within a dram in order to convey data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. and Keeth memory circuit elements to include the sense amplifiers as taught by Sato et al., since the modification is merely a substitution of a functionally recognized equivalent element. Further, the sense amplifiers of Sato et al. not only improve the performance of the device, but also a

necessity for the functionality of the device. Additionally, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

8. Claims 185 and 186 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011] and Zagar et al. [U.S. Patent # 5,761,145].

Hilley et al. disclose, in the figures and specification, a control unit for performing a series of instructions [memory controller - figure 2]; and a dynamic random access memory responsive to said control unit [banks coupled to the memory controller], said memory comprising: an array of memory cells [see figures 2-4]; a plurality of peripheral devices [see figure 5] for writing data into said memory cells and for reading data out of aid memory cells; and test mode logic [scan control] for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit [circuits coupled to RAS of figure 5] responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements [via odd or even], and an enable circuit [circuits coupled to R/W] responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements [via even or odd]. Additonally, Keeth disclose, as stated above, a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by

said array and said plurality of peripheral devices. Further, there exist rows and columns within the individual arrays within the memories of both Hilley et al and Keeth.

Hilley et al. and Keeth disclose all of the above mentioned but is silent about the fact that the dram has a capacity of 256 meg and that there exists redundant arrays to replace any defective cells. However, this is not new. Zagar et al. disclose that it is well known to have a dram with a capacity of 256 meg as well as corresponding redundant cells to replace any defective normal cells. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. and Keeth memory circuit elements to include the memory capacity as taught by Zagar et al., since the modification is merely a substitution of a functionally recognized equivalent element. Additionally, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

9. Claims 120, 187 and 188 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hilley et al. [U.S. Patent # 5,555,249] in view of Keeth [U.S. Patent # 5,651,011].

With respect to claim 120, Hilley et al. disclose, in the figures and specification, A combination for use in a memory having an array of memory elements, said combination comprising: test mode logic [scan controller – see figure 5] for determining whether the memory is in a test mode; a latching circuit [circuit coupled to ras]

responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements [via odd or even]; and an enable circuit [circuit coupled to R/W] responsive to a second external signal when the memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

Hilley et al. disclose all of the above mentioned but is silent about the fact that there's an actual entry step of testing mode. However, this is not new. Keeth disclose that it is well known to have a plurality of testing mode being initiated in order to test a memory device. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Hilley et al. memory circuit element's testing method to include the testing parameters as taught by Keeth, since the modification is merely a substitution of a functionally recognized equivalent element. Further, it is noted that it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. In re Karlson, 136 USPQ 184.

With respect to claim 187, both Hilley et al. and Keeth disclose said first external signal includes a row address strobe signal [RAS].

With respect to claim 188, both Hilley et al. and Keeth disclose said second external signal includes a column address strobe signal [CAS].

Allowable Subject Matter

10. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to other elements in the claim) the following:

- writing the latched test data into subsequent groups of memory elements in response to a second external signal; reading the test data from the subsequent groups of memory elements; and comparing the test data read from the subsequent groups of memory elements with the test data written to the first seed row of memory elements.

- each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

- array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

- said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

- a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

- additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

Conclusion

11. When responding to the Office action, Applicants are advised to provide

the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

13. Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
December 19, 2007